EMC Level 0Trigger

A review

Definitions

- EMC tower: 0.05x0.05 unit in Barrel geometry. Signal generated by PMT
- Trigger patch: 4x4 patch with 0.2x0.2 coverage generated in hardware from EMC towers
- High tower: Highest EMC tower in Trigger patch generated in hardware
- Jet patch: 1.0x1.0 patch generated from Trigger tower patches in Level 0 trigger
- All Signals are in E_t

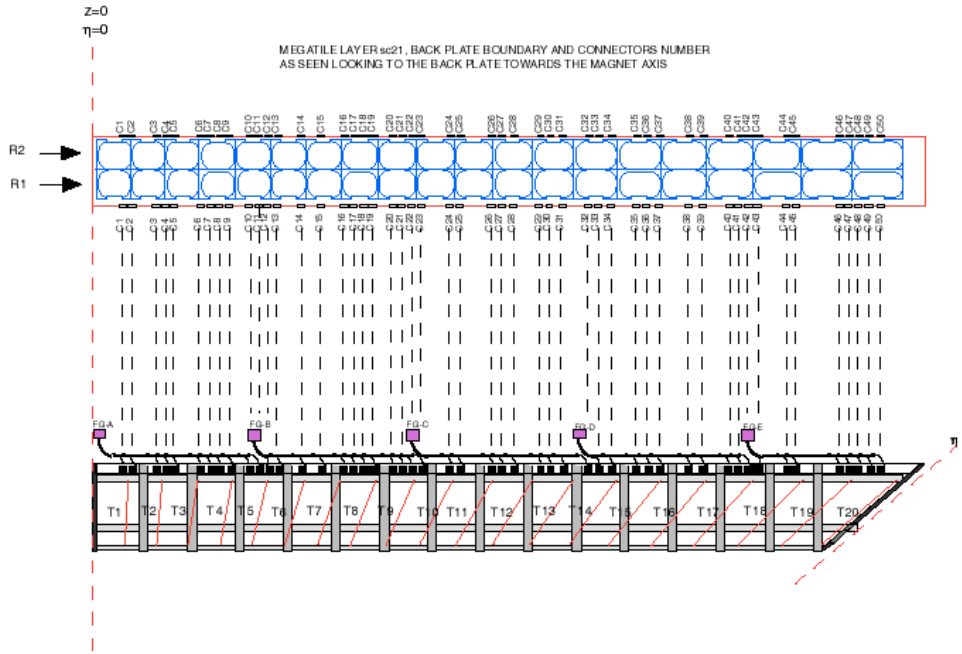
EMC Trigger Requirements

- See http://www.star.bnl.gov/STAR/html/trg_l/EMC/Requirements/emcreq.pdf
- Three selectable levels of Trigger on
  - Trigger patch
  - High tower
  - Ratio of High/Trigger tower -Not used this year
  - Jet patch
  - Total E_t
  - Counter ???

PreTrigger Components

- PMTs adjusted to give E_t
- ADC generate 12 bits
  - Upper 10 ten bits used for trigger
    - Top 8 for Trigger patch
    - User selects upper or lower 6 bits of 10 for High tower
- Individual PMTs maskable
- No other user options
- 300 Trigger patch/High tower pairs generated with 6 bits each (x2)

IDENTIFICATION OF COMPONENTS FOR ROUTING AND TAGGING
WSU, EMC, 3/5/99, JOSE RISO



SIDE VIEW OF THE EMC MODULE SHOWING THE NUMBER AND POSITION OF CONNECTORS IN RELATION TO TOWERS AND STRAPS, ALSO IS SHOWN THE POSITION OF THE FIBER GUIDES IN RELATION TO THE OPTICAL CONNECTORS AND NUMBER OF FIBER BUNDLES ROUTED THROUGH EACH GUIDE.

To give one example of how we can follow routing paths of fiber bundles let's suppose that we want to identify the route of a fiber or fiber bundle that starts at the photomultiplier box PMB# and finishes in tower T4 (Tower 4) in R1 (Row 1) of the module M60.

The path is:

PMB#>FG30BW>R1>C#>T4

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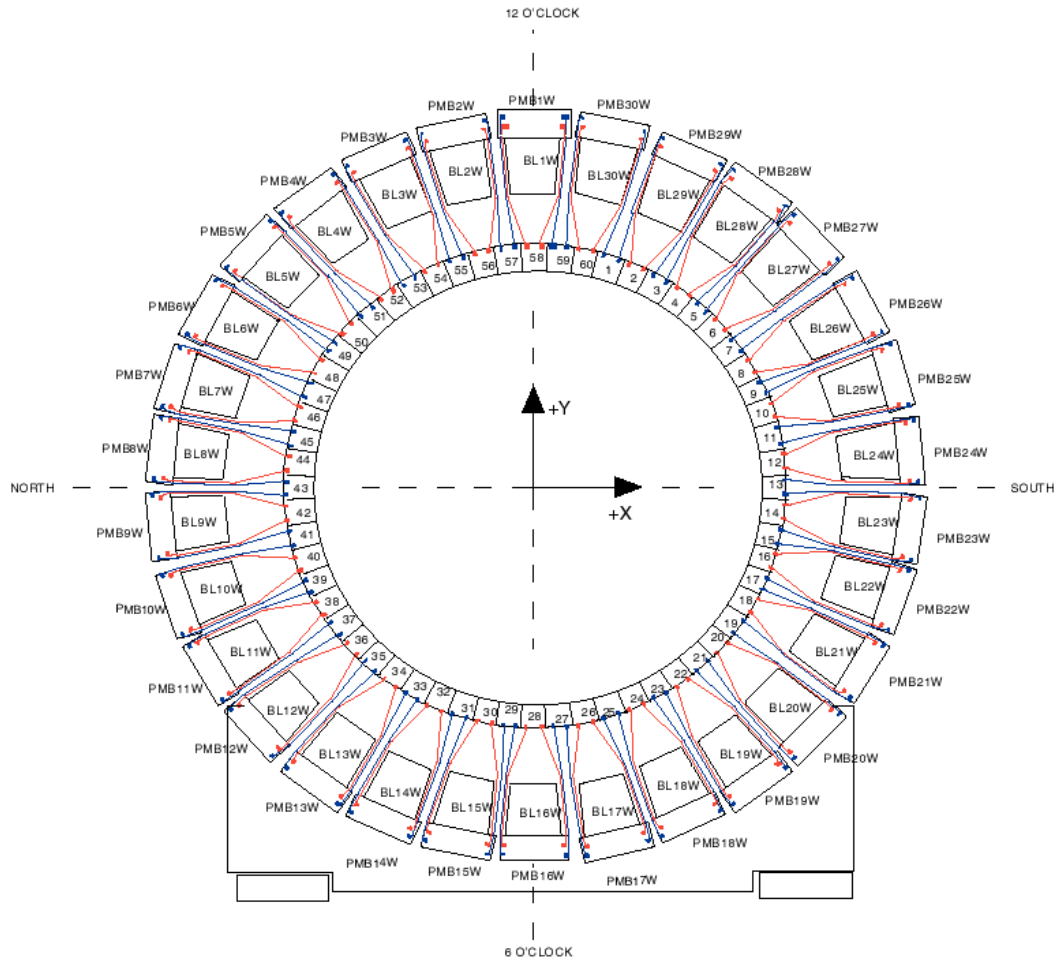
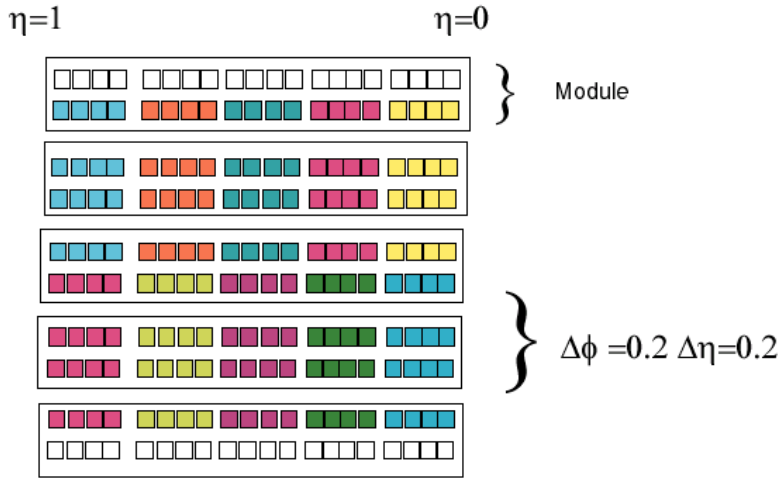
ROUTING AND TAGGING NAMING CODE
EMC, WSU, JOSE RISO, 10/26/99



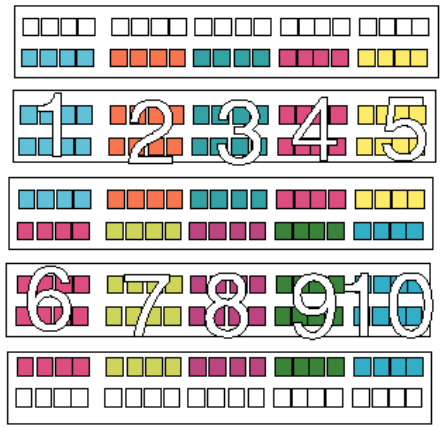
EMC FACE OF THE STAR BARREL AS SEEN FROM +Z (WEST FACE) SHOWING THE DISTRIBUTION OF PMT'S BOXES AND CLEAR FIBER BUNDLES

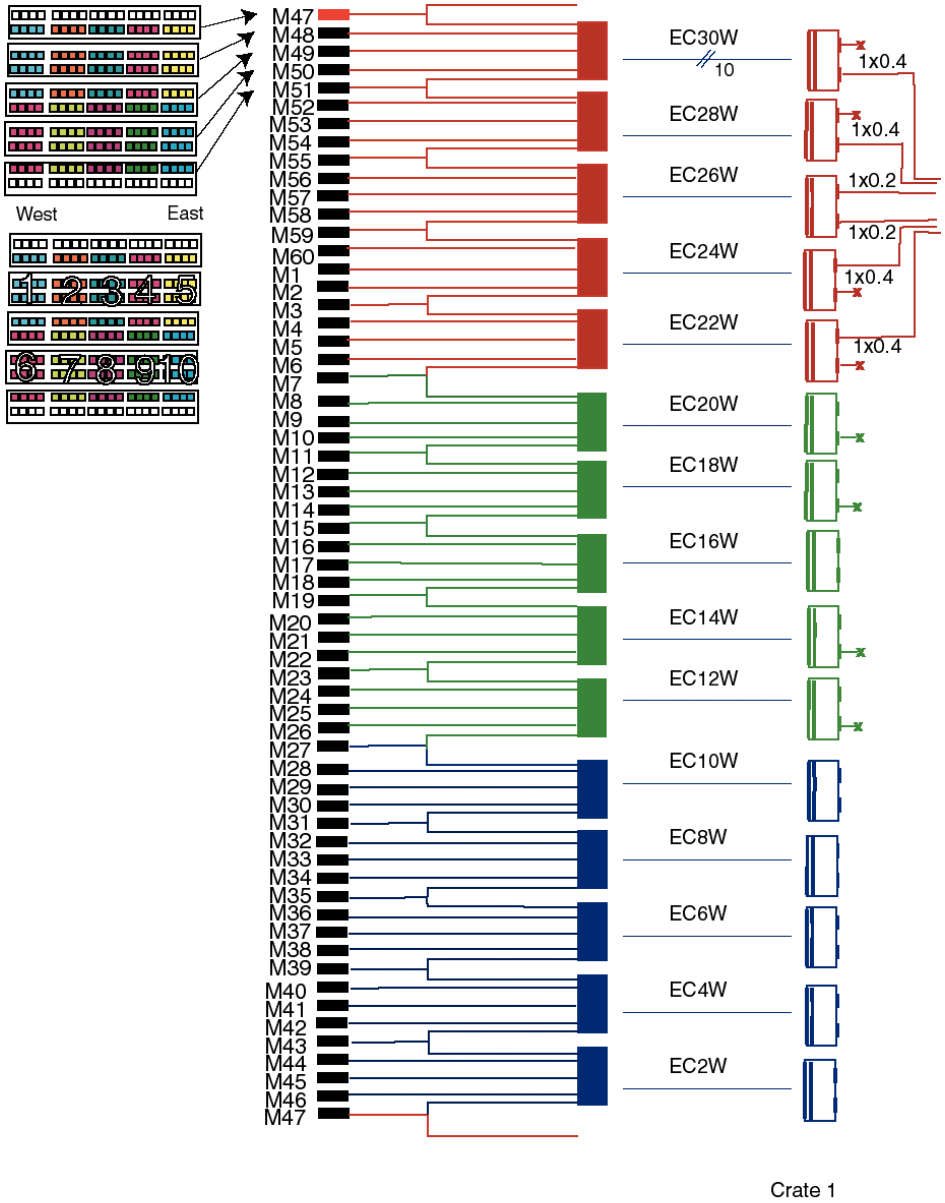


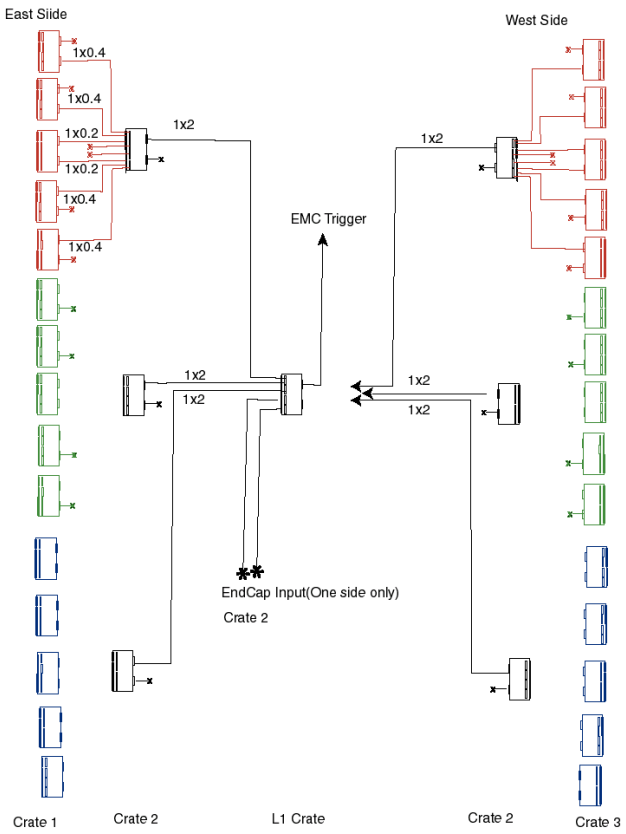
West

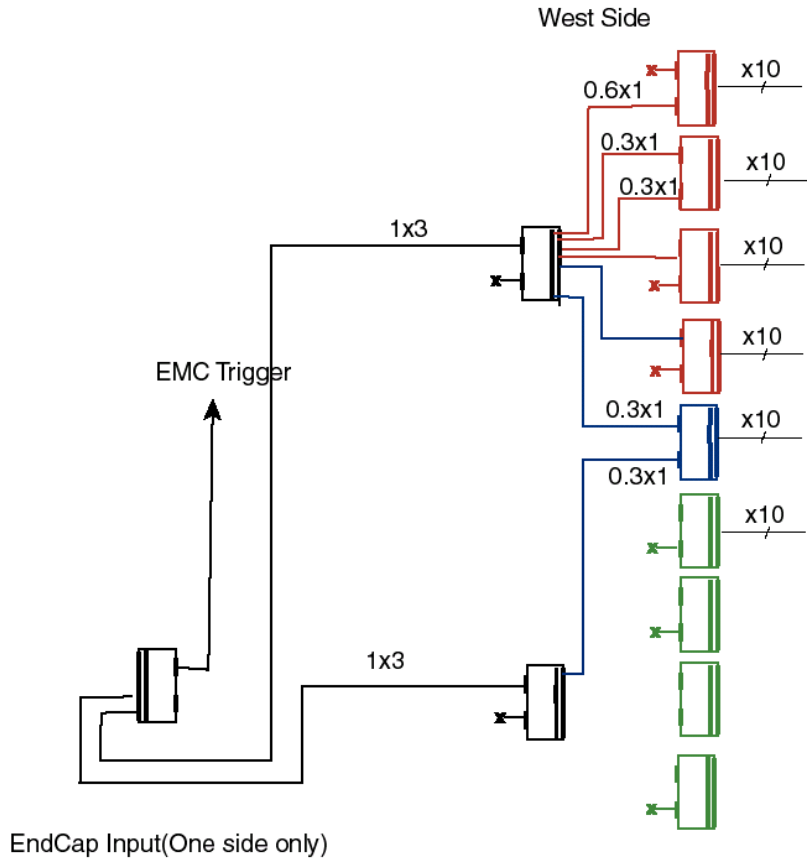
East

Layout of the Ten Trigger Towers




West
East
1 2 3 4 5
6 7 8 9 10
M47
M48
M49
M50
M51
M52
M53
M54
M55
M56
M57
M58
M59
M60
M1
M2
M3
M4
M5
M6
M7
M8
M9
M10
M11
M12
M13
M14
M15
M16
M17
M18
M19
M20
M21
M22
M23
M24
M25
M26
M27
M28
M29
M30
M31
M32
M33
M34
M35
M36
M37
M38
M39
M40
M41
M42
M43
M44
M45
M46
M47
EC30W
10
EC28W
EC26W
EC24W
EC22W
EC20W
EC18W
EC16W
EC14W
EC12W
EC10W
EC8W
EC6W
EC4W
EC2W
1x0.4
1x0.4
1x0.2
1x0.2
1x0.4
1x0.4
Crate 1


East Siide
West Side
1x0.4
1x0.4
1x0.2
1x0.2
1x0.4
1x0.4
1x2
1x2
EMC Trigger
1x2
1x2
1x2
1x2
**
EndCap Input(One side only)
Crate 2
Crate 1
Crate 2
L1 Crate
Crate 2
Crate 3



EndCap EMC Trigger Tree

Level 0 Trigger-Layer 1

- 30 TDSMI/DSM
  - 10 pairs of inputs
- High tower thresholds checked (2 bits out)
  - Implies order of requested levels
- Trigger patch thresholds checked (2 bits out)
- Ratios generated and thresholds checked (2 bits out) -Not used this year
- 1.0x0.4 patches generated (10 bits out)
  - OR 2 1.0x0.2 patches(every third)

Level 0 Trigger-Layer 2

- 6 DSMs with input of
  - 4 1.0x0.4 patches
  - 2 1.0x0.2 patch
  - 5 sets of 6 bits of threshold information
- OR threshold information (6 bits out)
- Generate 2 Jet patches and check thresholds (2 bits out)
- Generate Total E_t (8 bits out)

Level 0 Trigger-Layer 3

- 1 DSM with input of
  - 6 1.0x 2.0 P_t patches
  - 6 sets of 8 bit thresholds
  - EndCap
- OR threshold bits
- Generate Total E_t and check thresholds

Level 3 Output

- The output bit To STAR trigger
  - 10 bits (default) 8 used this run
    - 2 High Tower
    - 2Trigger Patch
    - 2 Jet Patch
    - 2 Total E_t
  - EndCap 10 bits(default) 8 used this run
    - Ibid

Status

- Hardware being installed
  - DSM/TDSMI installed and being cabled
  - Electronics Crates being installed
- Code
  - Single threshold High tower version implemented
  - New code to be written